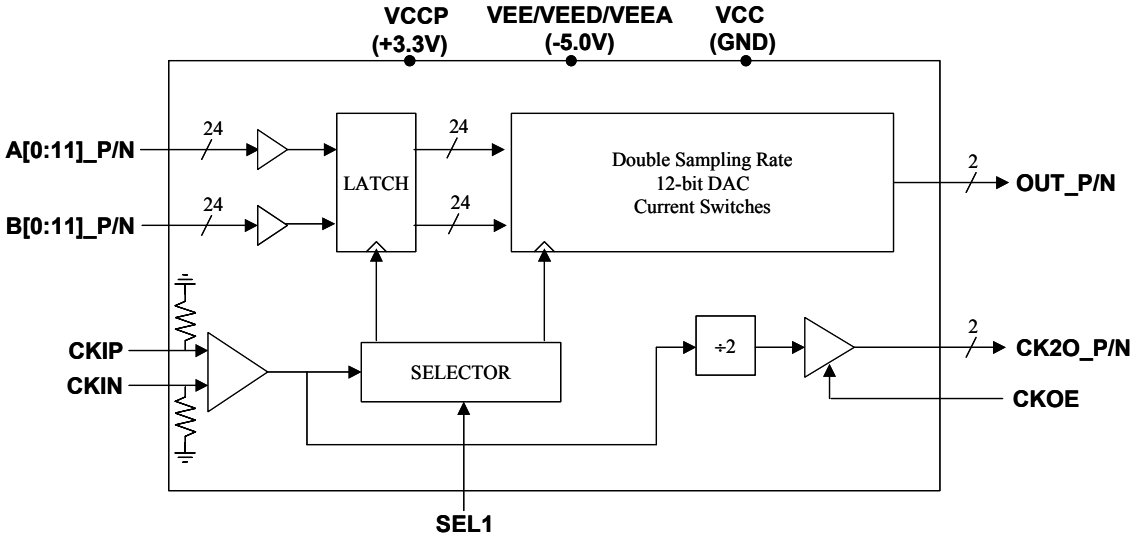
MD622H – Double Sampling Rate > 8 Gsps *MUXDAC*



Key Features

- 2:1 multiplexing ratio for each input bit of DAC
- Double Sampling Rate (DSR) DAC enables analog output sampling rate twice of the clock rate
- Clock rate up to > 4 GHz with DAC analog output > 8 Gsps
- Complementary outputs with 50-Ω back terminations
- Complementary divided-by-2 clock LVDS outputs for data synchronization
- Divide-by-2 clock output drivers with enable/disable control without interrupting internal operations of the chip
- On-chip 100 ohm termination between each differential LVDS input data and RESET pair
- 2.7W power consumption
- QFN 10x10 88L package with exposed pad

Applications

- Arbitrary waveform generation
- Radar/Ladar design and testing
- Software defined radio
- Electronic warfare
- Wireless basestations
- RF signal source generation
- Hard disk and magnetic storage testing
- WLAN testing
- Advanced communication modulations

Description

The **MD622H** is a high-speed 12-bit Digital to Analog Converter (DAC) integrated with 2:1 multiplexer for each DAC input bit. The digital data inputs are LVDS with on-chip 100 ohm termination resistors. The Double Sampling Rate (DSR) DAC enables its analog output sampling rate twice of the clock rate. The device can be clocked up to > 4 GHz to achieve > 8 Gsps at DAC outputs. To minimize the glitch energy and to achieve high linearity, the DAC is based on a 4-bit segmented with 8-bit R-2R architecture. Complementary outputs are available with 50-Ω output back terminations. Divided-by-2 clock LVDS outputs (**CK2O_P/N**) and sampling phase selection (**SEL1**) are provided to ease the alignment of sampling phase relative to the input data. **CKOE** pin is provided to enable/disable output drivers of **CK2O_P/N** clock outputs without interrupting the internal operations for the convenience of system applications.