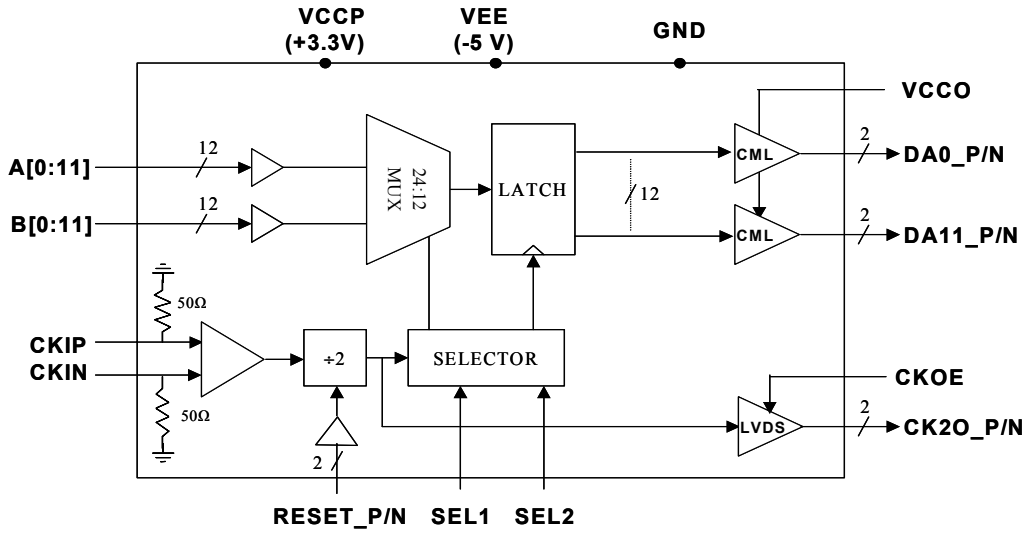
MX2412D – 4 Gbps 12-Bit 2:1 Multiplexers



KEY FEATURES

- 12 bit 2:1 (total 24:11) multiplexers with each differential output bit operates > 4 Gbps
- Designed for additional data multiplexing needed for ***Euvis*** > 8 Gsps MUXDACs such as **MD622H** and **MD662H**
- On-chip 100 ohm termination between each differential LVDS input data and **RESET** pair
- 12 bit differential pair outputs with pull-up power supply **VCCO** to match various high speed interface standards
- Optimal input data sampling window selections (**SEL1/SEL2**)
- Complementary divided-by-2 clock LVDS outputs with output driver enable/disable control (**CKOE**) without interrupting internal operations of the chip
- **RESET** function to synchronize multiple chip applications
- 2.2 W power consumption
- QFN package with Exposed Pad to enhance grounding and heat dissipation

Description

The **MX2412D** is a high-speed 12-channel of 2:1 multiplexers. The 24 differential pair data inputs were multiplexed to 12 bit differential data outputs. The pull-up power supply **VCCO** of output drivers can be used to set the output level suitable for most popular high-speed interface standards such as CML or LVDS. The multiplexer can be operated at a clock rate > 4 GHz. The digital data inputs are LVDS with on-chip 100 ohm termination resistors. Control pins **SEL1/SEL2** select the optimal sampling windows to accommodate various delays of the 48 pair input data. Divided-by-2 clock outputs **CK2O_P/N** and sampling phase selection (**SEL1** and **SEL2**) are provided to optimize the alignment of sampling phase relative to the input data. A **RESET** function is provided for applications which need to synchronize the outputs from multiple **MX2412D** chips. **CKOE** pin is provided to enable/disable output driver of **CK2O_P/N** clock outputs without interrupting the internal operations for the convenience of system applications.

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