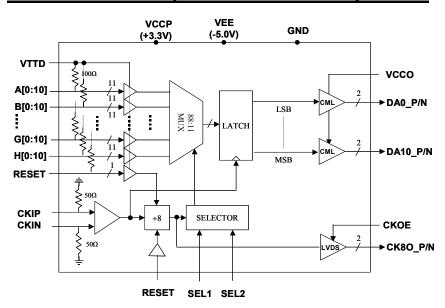
## MX8811S - 4 Gbps 11-Bit 8:1 Multiplexers



## **KEY FEATURES**

- 11 bit 8:1 (total 88:11) multiplexers with each differential output bit operates > 4 Gbps
- Designed for additional data multiplexing needed for *Euvis* > 8 Gsps MUXDACs such as MD622H and MD662H
- On-chip 100 ohm termination to VTTD for single-ended data and RESET inputs
- 11 bit differential pair outputs with pull-up power supply **VCCO** to match various high speed interface standards
- Optimal input data sampling window selections (**SEL1/SEL2**)
- Complementary divided-by-8 clock LVDS outputs with output driver enable/disable control (**CKOE**) without interrupting internal operations of the chip
- **RESET** function to synchronize multiple chip applications
- 2.7 W power consumption
- TQFP package with Exposed Pad to enhance grounding and heat dissipation

## Description

The MX8811S is a high-speed 11-channel of 8:1 multiplexers. The 88 single-ended data inputs were multiplexed to 11 bit differential data outputs. The pull-up power supply VCCO of output drivers can be used to set the output level suitable for most popular high-speed interface standards such as CML or LVDS. The multiplexer can be operated at a clock rate > 4 GHz. The digital data inputs are single-ended with on-chip 100 ohm termination resistors to its reference voltage VTTD which can tolerate a wide range voltage level suitable for various single-ended interface standards. Control pins SEL1/SEL2 select the optimal sampling windows to accommodate various delays of the 88 input data. Divided-by-8 clock outputs CK8O\_P/N and sampling phase selection (SEL1 and SEL2) are provided to optimize the alignment of sampling phase relative to the input data. A RESET function is provided for applications which need to synchronize the outputs from multiple MX8811S chips. CKOE pin is provided to enable/disable output driver of CK8O\_P/N clock outputs without interrupting the internal operations for the convenience of system applications.

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